ABSTRACT OF THE DISCLOSURE

A cycle slip detector interfaces with a phase/frequency detector (PFD), such as might be used in a phase-locked loop circuit (PLL), and indicates when cycle slips occur in the PFD. Typically, the PFD generates output control signals as a function of the phase difference between first and second input signals, with the first input signal usually serving as a reference signal against which the PLL adjusts the second input signal. The PFD provides linear phase comparison between its input signals, provided their relative phase difference does not exceed $\pm 2\pi$ radians. If one of the two signals leads or lags the other by more than that amount, a cycle slip occurs, and the PFD responds nonlinearly. The cycle slip detector provides logic for detecting and indicating leading and lagging cycle slips as they occur in the PDF, and is typically implemented as a minimal arrangement of logic gates and flip-flops.